REMARKS

Claims 1-14 and 27-30 are all the claims pending in the application. Claims 1-14 stand rejected on prior art grounds. Claims 15-26 have been canceled without prejudice or disclaimer. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-14 stand rejected under 35 U.S.C. §102(b) as being anticipated by Assaderaghi, et al. (U.S. Patent No. 5,759,907), hereinafter referred to as Assaderaghi. Claims 1-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Assaderaghi, in view of Adkisson, et al. (U.S. Publication No. 2002/0064913 A1), hereinafter referred to as Adkisson. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a silicon-on-insulator integrated structure comprising a decoupling capacitor ***outside*** of an active region. In the rejection, the Office Action argues that the claimed invention is anticipated by Assaderaghi or, in the alternative, is obvious over Assaderaghi in view of Adkisson. However, both Assaderaghi and Adkisson disclose a structure having a capacitor located ***inside*** of an active region. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

Both Assaderaghi and Adkisson disclose a capacitor located ***inside*** of an active region. More specifically, in regards to Assaderaghi, Assaderaghi forms a capacitor, that is not necessarily high value through the ***active*** structure above the shallow trench isolation in an SOI region, as correctly depicted starting in Assaderaghi Fig 3 where an N+ implant (16) is performed into open trench 18, that has been preformed through and adjacent to an active Si region 12. This implant then converts the Si region 12 to N+, as shown; later in figures 6 and 7. Assaderaghi then fills said trenches with N+ polysilicon. Assaderaghi relies on the dopant diffusion of implant (16) to provide a highly conductive plate as described by Fig 7. The active Si regions between the trenches (17) are then doped through diffusion of the implanted species. This is captured in Assaderaghi claim 1, ... forming capacitor structures extending through said silicon layer and said buried insulating layer and into said semiconductor structure..... implanting second dopant type...into "portions" of said semiconductor substrate located beneath said trench bottoms...

Additionally, as noted in paragraph 30 of Adkisson, the DRAM array 24 comprises active areas. Further, as illustrated in Figure 3, capacitor trenches 32 are formed in this region comprising active areas. Moreover, as described in paragraphs 29 and 30 of Adkisson, the formation of the remainder of the storage capacitors and the vertical gates in the DRAM array 24 is next performed, as illustrated in FIG. 4. All of the deep trenches 32 are filled with doped polysilicon 45, which serves as the inner electrode of the trench capacitor. The layer of doped polysilicon 45 within each deep trench 32 is then recessed. The top part of the collar is removed with a wet etch (e.g., using

hydroflouric acid (HF)), strap connections between the doped polysilicon 45 and the crystalline bulk region 12 are formed, and a trench top oxide ("TTO") layer 40 is deposited upon each recessed doped polysilicon layer 45. A gate oxide is introduced into each diffusion region 43 in the DRAM array 24 to form the array gates 42. In the next step, polysilicon array gate conductor regions 44 are deposited on each deep trench 32, and their top surfaces are recessed using known etching methods. Elsewhere in the DRAM array 24, a BOX layer 14 covers each of the diffusion regions 43. A silicon oxynitride (SiON) layer 46 may grow on the upper surface of the nitride polish stop 20 during the various oxidation steps. A vertical nitride or polysilicon spacer 47 may build up between the DRAM array region 24 and the bulk region 26 during the various deposition and etch steps. Next, the active areas in the DRAM array are defined.

Unlike Assaderaghi and Adkisson, the claimed invention comprises a decoupling capacitor that is ***outside*** of the active region. Such a feature is defined in independent claims 1, 8, and 27 using the following language: "said decoupling capacitor is outside said active region". As illustrated in Figure 3A, the heavy vertical dashed line separates the active area 315 from the bulk silicon region 106, wherein the decoupling capacitor 200 is outside of the active region 315. Therefore, as more fully described above, both Assaderaghi and Adkisson teach away from the claimed invention by providing a capacitor that is inside of the active region.

Therefore, contrary to the position taken in the Office Action, Applicants submit that neither Assaderaghi nor Adkisson teach or suggest a decoupling capacitor that is ***outside*** of the active region. Thus, it is Applicants' position that neither Assaderaghi nor

Adkisson disclose or suggest the claimed feature, wherein "said decoupling capacitor is outside said active region" as defined by independent claims 1, 8, and 27.

Therefore, it is Applicants' position that the proposed combination of Assaderaghi and Adkisson do not teach or suggest many features defined by independent claims 1, 8, and 27 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2-7, 9-14, and 28-30 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-14 and 27-30, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any

deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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